IN THE CLAIMS

Amended claims follow. Insertions are underlined, while deletions are struck out. The status of each claim is included prior to each heading.

1. (Original) An integrated circuit, comprising:
an active circuit;
a metal layer disposed, at least partially, above the active circuit; and
a bond pad disposed, at least partially, above the metal layer;
wherein the metal layer is meshed.

2. (Original) The integrated circuit as recited in claim 1, wherein the active circuit includes an input/output (I/O) bus.

3. (Original) The integrated circuit as recited in claim 1, wherein the active circuit includes a plurality of transistors.

4. (Original) The integrated circuit as recited in claim 1, wherein the metal layer includes an interconnect metal layer.

5. (Original) The integrated circuit as recited in claim 4, wherein the interconnect metal layer interconnects the bond pad with a plurality of underlying metal layers.

6. (Currently Amended) The integrated circuit as recited in claim 5, wherein each of the underlying metal layers ~~are~~is in electrical communication by way of a plurality of vias.

7. (Original) The integrated circuit as recited in claim 1, wherein the metal layer includes a plurality of openings.

8. (Original) The integrated circuit as recited in claim 7, wherein the openings are adapted for facilitating an interlock between the metal layer and an inter-metal dielectric layer disposed between the metal layer and the bond pad.

9. (Original) The integrated circuit as recited in claim 8, wherein the inter-metal dielectric layer is constructed from a material selected from the group consisting of a low-K dielectric material and a fluorinated silica glass (FSG) material.

10. (Original) The integrated circuit as recited in claim 7, wherein the openings are completely enclosed around a periphery thereof.

11. (Original) The integrated circuit as recited in claim 7, wherein the openings have a substantially square configuration.

12. (Original) The integrated circuit as recited in claim 7, wherein the openings define a plurality of substantially linear first portions and a plurality of substantially linear second portions which intersect.

13. (Original) The integrated circuit as recited in claim 12, wherein the openings define a matrix of openings.

14. (Original) The integrated circuit as recited in claim 13, wherein a plurality of interconnect vias are formed in rows along the first portions.

15. (Original) The integrated circuit as recited in claim 14, wherein the interconnect vias are spaced along a length of the first portions.

16. (Original) The integrated circuit as recited in claim 15, wherein the interconnect vias include one single row for each of the first portions.

17. (Original) The integrated circuit as recited in claim 15, wherein the interconnect vias include at least two spaced rows for each of the first portions.

18. (Original) The integrated circuit as recited in claim 17, wherein a width of the first portions is enlarged to accommodate the at least two spaced rows for each of the first portions.

19. (Withdrawn)

20. An integrated circuit, comprising:

an active circuit means for processing electrical signals;

a metal layer disposed, at least partially, above the active circuit means and including a mesh means for preventing damage incurred during a bonding process; and

a bond pad disposed, at least partially, above the metal layer.

21. An integrated circuit, comprising:

a semiconductor structure including an active circuit including an input/output (I/O) bus and a plurality of transistors forming a core of circuits;

a plurality of vertically spaced underlying metal layers disposed, at least partially, under the active circuit and around a periphery thereof, wherein each of the underlying metal layers are in electrical communication by way of a plurality of underlying vias with the active circuit and other underlying metal layers;

a meshed interconnect metal layer disposed, at least partially, above the I/O bus of the active circuit and around a periphery thereof, the interconnect metal layer being in electrical communication with the underlying metal layers by way of a plurality of additional vias;

an inter-metal dielectric layer disposed, at least partially, above the interconnect metal layer, the inter-metal dielectric layer constructed from a material selected from the group consisting of a low-K dielectric material and a fluorinated silica glass (FSG) material;

a top metal layer disposed, at least partially, above the inter-metal dielectric layer, the top metal layer for serving as a bond pad, the top metal layer being in electrical communication with the interconnect metal layer by way of a plurality of interconnect vias; and

a passivation layer disposed, at least partially, above the top metal layer.

wherein the interconnect metal layer is meshed for preventing damage incurred during a bonding process.

22.- 26. (Withdrawn)

27. (New) The integrated circuit as recited in claim 1, wherein the metal layer is disposed, at least partially, above the active circuit along a vertical axis.

28. (New) The integrated circuit as recited in claim 1, wherein the metal layer is disposed, at least partially, directly above the active circuit.

29. (New) The integrated circuit as recited in claim 8, wherein the inter-metal dielectric layer is constructed from a low-K dielectric material.

30. (New) The integrated circuit as recited in claim 8, wherein the inter-metal dielectric layer is constructed from a fluorinated silica glass (FSG) material.

31. (New) The integrated circuit as recited in claim 1, wherein the mesh ensures that bonds are capable of being placed over the active circuit without damage thereto during a bonding process.